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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/730,533	12/07/2000	Hideyuki Shimonishi	040405/0330	9357
22428	7590	09/28/2004	EXAMINER	
FOLEY AND LARDNER			PAN, DANIEL H	
SUITE 500			ART UNIT	PAPER NUMBER
3000 K STREET NW				2183
WASHINGTON, DC 20007			DATE MAILED: 09/28/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/730,533	SHIMONISHI, HIDEYUKI
	<b>Examiner</b>	<b>Art Unit</b>
	Daniel Pan	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 07 December 2000.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-46 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-7 and 28-30 is/are rejected.  
 7) Claim(s) 8-27,31- 46 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 07 December 2000 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>3</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____ .

1. Claims 1-46 are presented for examination.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2,4-7 are rejected under 35 U.S.C. 102(a) and (b) as being anticipated by Saito et al (5,784,630).

3. As to claim 1, Saito disclosed a system including at least :

a) dividing a group of processors [ALUs] constituting a microprocessor system into a plurality of groups [A2][A3] of processing elements (see fig.3B [ALU1] and [ALU2] or [[ALU3] and [ALU4], see fig.3A for the plurality of groups A1 and A2);

b) conducting interprocessor communication by physically shared a same register [D15] among processors [ALU1] [ALU2] belong to the same processing element [A2] ;

c) conducting interprocessor communication directly transferring the content of the register file [D15] through a bus [D5 global bus] to processor [ALU3][ALU 4] belong to different processing elements (see how the data content in register file D15 read out to A3, see how the D15 register file was shared by other processing element s in col.11, lines 10-23, col.14, lines 24-28).

4. As to claim 2, Saito also included one to one channel for each register (e.g. see col.11, lines 49-55).

5.

6. AS to claims 4, 5, Saito also included communication between processing elements belong to the same group through ten same bus [d1] (see fig.3B, A2) and communication belong to different group using a bridge [gate D17 ] (fig.3B, see the D17 gate on global bus in col.14, lines 44-51).

7. AS to claim 6, Saito also include no less than one route[D17] connecting processing elements (see fig. 3B);

8. As to claim 7, Saito also included not less than one global bus [d2] , and not less than one route [D17] (see fig.3 B).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al (5,784,630) in view of Ishida et al. (5,293,500).

10. As to claim 3, limitations of the parent claim have been discussed in paragfraph # 3 above, therefoe, it will not be repeated herein. Saito did not specifically showed the sharing of the channel with the registers in the register file as claimed. However, Ishida disclosed a system including a plurality of registers [registers] in a register file for

sharing a channel [17] (e.g. see fig.4). It would have been obvious to one of ordinary skill in the art to use Ishida in Saito for including the sharing of the channel as claimed because ht use of Ishida could provide Saito to control ability to adjust to different number of register at a predetermined number of channel , increasing the ability of Saito's register to adapt to specific number of channel at a given current cycle, and therefore reducing the circuit overheads of the extra connections, and it could be readily done by configuring the channel connection of Ishida into Saito with modified control parameters , such as the channel number and width, so that the shared channel of Ishida could be recognized by Saito in order to provide the enhanced shared structure, and for the above reasons , provided a motivation.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 28-30 are rejected under 35 U.S.C. 102(a) and (b) as being anticipated by Ishida et al (5,293,500).

12. As to claim 28, Ishida included at least :

a) a plurality of processing elements [processing units], each including a plurality of processors (see fig.6 for the structure of a processing unit which included the integer

and floating point processors) sharing the same register file [register file ] (see fig.6 [register file]);

b) a bus structure formed of a local bus (see fig.4) for connecting register files (see fig.4 register files 12, 13) ) of several processing elements [11][15] , not less than one global bus (17) for connecting to local buses (see the respective connections to each register in fig.4) and not less than one bridge (e.g. see the relay [31]) for relaying data between the buses.

13. As to claim 29, Ishida also included one to one channel (see respective connections to each register in fig.,4).

14. AS to claim 30, each channel (see input 2 connections to 31) had the number smaller than the number of registers in register file (see fig.4).

15. Claims 8-13,26,27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the route causing no time contention on the same bus with other routes and the time of use determined in advance to time divisionally use the buses, and conducting the interprocessor communication using the determined route and time of use.

16. Claims 14-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further

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teaches the combined features of the route causing no contention on the same channel of the same bus with other routes was determined in advance to space-divisionally use the buses on a channel basis, and conducting only interprocessor communication using the determined route.

17. Claims 19-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the route causing no contention on the same channel of the same bus with other routes and a time of use of a channel of each bus by each route was determined in advance to space-divisionally use the buses on a channel basis, and conducting only interprocessor communication using the determined route.

18. Claims 31,32,43-46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the detailed functional elements of time table in each register file and the time table in each router.

19. Claims 33-36,39,40-42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior of record teaches the combined features of the detailed functional elements of connection table in each register file and the connection table in each bridge.

20. Claims 37,38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the detailed functional elements of time table in each register file and the time table in each bridge.

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a). Hahn et al. (6,108,766) is cited for the basic teaching of the plurality of processing elements including a plurality of processors with respective shared register files (see fig.2, see col.5, lines 15-51).

b) Davie (6,320,845) is cited for the background teaching on routing circuitry based on the time constraints or contentions (see col.2, lines 10-66);

c) Van Meerbergen et al. (5,613,152) is cited for the teaching of register files of respective processing units (e.g see col.5, lines 14-53).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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